10-03-07

PATENT
Attorney Docket No. 9145.0021-00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
TZONG-KWANG HENRY YEH et al.	Group Art Unit: 2189
Application No.: 10/808,253	Examiner: FLOURNOY, Horace L.
Filed: March 23, 2004	
For: COLLISION DETECTION IN A MULTI-PORT MEMORY SYSTEM	Confirmation No.: 4222

MAIL STOP PETITION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PETITION TO WITHDRAW ERRONEOUS HOLDING OF ABANDONMENT BASED ON FAILURE TO SUBMIT CORRECTED DRAWINGS

Pursuant to 37 C.F.R. § 1.181(a), Applicants hereby petition the Commissioner for Patents to withdraw the holding of abandonment of this application based on the alleged failure to submit corrected drawings. Because the error was made by the Patent Office, Applicants believe that no fees are due.

Applicants were informed of the abandonment status after checking on the particulars of the provisional application. After speaking with a representative with the EBC Customer Service Center, we were informed that the reason for abandonment was the "failure to timely submit corrected drawings to the Notice of Allowance mailed on May 1, 2007." In May, 2007, the undersigned Applicants' representative, contacted the Examiner by telephone and he indicated that Box No. 5 for Corrected Drawings was checked in error, and no submission of corrected drawings was required. We subsequently requested a Corrected Notice of Allowance and the Examiner indicated that there was no guarantee that one would be issued. As a result, Applicants paid the issue fee in the application without re-submitting the already accepted drawings. As of

today, we have not received the corrected Notice of Allowance or a Notice of Abandonment by mail.

In addition, the Examiner indicated in the Office Action mailed March 24, 2006, that the drawings filed on March 23, 2004, were accepted (for convenience, a copy of this Office Action is attached). The status of the drawings were not addressed in any subsequent communications from the PTO afterward until the mailing of the Notice of Allowance. Further, in addition to our telephone conversation with the Examiner confirming that Box No. 5 for Corrected Drawings was checked in error, the Examiner's Statement of Reasons for Allowance made no mention of corrected drawings being required (for convenience, a copy of the Notice of Allowance is attached).

Accordingly, Applicants respectfully request that the Commissioner of Patents grant this petition to withdraw the holding of abandonment of this application, and place this application in condition for grant.

If any additional fees are due in connection with the filing of this Petition, including any fees required for an extension of time under 37 CFR § 1.136, such an extension is requested, and the Commissioner is authorized to charge any required fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

By: _____
Gary J. Edwards
Reg. No. 41,008

Dated: October 1, 2007

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,253	03/23/2004	Tzong-Kwang Henry Yeh	9145.0021-00	4222

22852 7590 03/24/2006

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EXAMINER	
FLOURNOY, HORACE L	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

3/27/06

Docketed 3-27-06 Attorney CLO-GJG
Case 9145-0
Due Date: 6-24-06 of eff
Action Voy Office Ltr
By

Office Action Summary

Application No.	Applicant(s)	
10/808,253	YEH ET AL.	
Examiner	**Art Unit**	
Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/15/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. **10/808,253** has a total of *15* claims pending in the application; there are *5* independent claims and *10* dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required by **M.P.E.P. 201.14(c),** acknowledgement is made of applicant's claim for priority based on an application filed on February 26, 2004 (Provisional Application # 60/548,527).

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

As required by **M.P.E.P.** 609(c), the applicant's submission of the Information Disclosure Statement dated **09/15/2005** is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P.** 609(c), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by **Luo et al. (U.S Patent No. 6,169,700 hereafter referred to as Luo)**.

With respect to **independent claim 1,**

> *"A multi-port memory system,* **[Luo discloses in the abstract, "dual port device"]** *comprising: a memory array with an addressable array of memory locations: at least two ports coupled to the memory array,* **[Luo discloses this limitation e.g. in the abstract, "An asynchronous wait state generator circuit and method is included in a dual port device, e.g., in a dual port memory, to allow the use of separate address decoders and simultaneous access to memory locations from asynchronously operating, separate ports. "]** *each of the at least two ports transmitting to the memory array an address, a clock signal,* **["clock signal" disclosed in the abstract]** *and a read/write control signal;* **[Luo discloses in column 4, lines 4-8, "Conventional addressing, read/write and other control signals associated with the**

respective address and data buses are not shown for simplicity of explanation. "] *and a collision detect circuit coupled to receive the address, the clock signal, and the read/write control signal from each of the at least two ports,* **[Luo discloses these limitations, e.g. in FIGs. 1-3 and associated text]** *wherein the collision detect circuit sets a collision flag* **["SAME_LOC"]** *when a collision condition is detected in any of the at least two ports."* **[Luo teaches this limitation, e.g. in column 4, lines 50-56, "If the two simultaneous addresses indicate a collision would occur in an access to the same address location, a same location signal SAME_LOC is activated, e.g., goes to a logic HIGH state for the duration of the collision of address signals. Otherwise, the same location signal SAME_LOC remains inactive, e.g., at a logic LOW state." Luo also discloses this limitation in column 6, line 67 – column 5, lines 1-5]**

With respect to **claim 2**,

"The system of claim 1, further including control logic coupled to the memory array **[disclosed, e.g. in FIG. 1 and column 1, lines 23-26]** *to receive signals associated with the at least two ports* **[Luo discloses in the abstract, "dual port device"]** *and present signals to the memory array."* **[Luo discloses this limitation, e.g. in the abstract, "a wait state signal is generated for the relevant port having the later attempt to access the same memory or other addressable location."]**

With respect to **claim 3**,

"The system of claim 1, wherein the collision detect circuit sets the collision flag associated with one of the at least two ports if another of the at least two ports is executing a write operation to a memory location at the same that that the one of the at least two ports accesses the memory location." **[Luo discloses in column 4, line 67 – column 5, lines 1-5, "...when the two simultaneous addresses are the same, and at least one of the operations is a write access, an access collision occurs. In such a case, a wait state signal is preferably generated to halt one of the processors or other addressing devices communicating with the respective ports of the dual port device."]**

With respect to **claim 4**,

"The system of claim 1, wherein the collision detect circuit comprises: an address compare circuit coupled to receive and compare addresses from each of the at least two ports and provide a match signals indicating which of the addresses are the same; **[Luo teaches this limitation, e.g. in column 4, lines 50-56, "If the two simultaneous addresses indicate a collision would occur in an access to the same address location, a same location signal SAME_LOC is activated, e.g., goes to a logic HIGH state for the duration of the collision of address signals. Otherwise, the same location signal SAME_LOC remains inactive, e.g., at a logic LOW state."]** *and at least one collision detect logic coupled to receive the match signals and the read/write signals and provide a collision signal for a first port of the at least two ports if the match signals indicate an address match between the first port and a second port of the at least two*

ports and the read/write signal associated with the second port indicates a write operation; **[Luo discloses in column 4, lines 57-61, "The asynchronous, simultaneous access wait state generator 123 generates a wait state signal WAIT STATE 1 relating to the first port of the dual port device, and a wait state signal WAIT STATE 2 relating to access from the second port of the dual port device. "]** *and at least one collision flag set circuit coupled to receive a collision signal from the collision detect logic* **["wait state generator 123"]***and set a collision detect flag according to the clock signal associated with the first port."* **[Luo discloses in column 5, lines 20-25, "...when a clock signal is at a logic HIGH), and the data is transferred, e.g., during the subsequent phase(0) (e.g., when the clock signal is at a logic LOW). Thus, when a collision is determined by the simultaneous access determination module 120 (e.g., when the same location SAME_LOC signal is activated)..."]**

With respect to **claim 5**,

"The system of claim 4, wherein the collision flag set circuit associated with the first port comprises: a flip-flop circuit that is set according to the collision detect flag; **[FIG. 4 and associated text e.g.]** *a first latch that latches an output signal from the flip-flop circuit on a rising edge of the clock signal associated with the first port; a second latch that latches a signal from the first latch* **["The first meta-stable wait state generator circuit 397 includes a meta-stable D-type Flip-Flop 310a (DFF), and the second meta-stable wait state generator circuit 399 includes another meta-stable DFF 310b." The examiner interprets a D Flip Flop as analogous to a latch. See FIGs. 3-4]** *on a falling edge of the clock*

signal associated with the first port; **[Luo discloses in column 5, lines 20-25, "...when a clock signal is at a logic HIGH), and the data is transferred, e.g., during the subsequent phase(0) (e.g., when the clock signal is at a logic LOW). Thus, when a collision is determined by the simultaneous access determination module 120 (e.g., when the same location SAME_LOC signal is activated)..."]** *and an output driver coupled to receive a signal from the second latch and provide a collision detect flag."* **[FIG. 1, elements 110, 120, and 123]**

With respect to **claim 6**,

"The system of claim 5, wherein the flip-flop circuit is reset from the signal from the first latch." **[Luo discloses in column 6, lines 6-10, "The clear signal to the first meta-stable DFF 310a is provided by a NORed combination of the reset signal RESET and an ANDed combination of the WAIT STATE 1 and WAIT STATE 2 signals using a NOR gate 320 and an AND gate 330." See FIG. 4]**

With respect to **claim 7**,

"The system of claim 5, further including a first-in-first-out circuit to store addresses in response to the collision signal." **[This claim is taught by Luo in column 5, lines 15-30. Luo discloses that the circuit which maintains the WAIT STATE signals, utilizing the clock signal, can apply a particular**

accessing processor for retrieving addresses in the order in which it is received. The signals are stored in the circuit.]

With respect to **independent claim 8**,

"A dual port memory system, comprising: a memory array coupled to receive a left port memory address and a right port memory address; **[FIG. 1, elements "FROM ADDR 1, FROM ADDR 2, DATA 1, and DATA 2"]** *and a collision detect circuit* **[FIG. 1, elements 110, 120, and 123]** *configured to detect a match between the left port memory address and the right port memory address and generate a left port collision flag if the right port is writing data, and generate a right port collision flag if the left port is writing data."* **[Luo discloses in column 4, lines 57-61, "The asynchronous, simultaneous access wait state generator 123 generates a wait state signal WAIT STATE 1 relating to the first port of the dual port device, and a wait state signal WAIT STATE 2 relating to access from the second port of the dual port device. "]**

With respect to **claim 9**,

"The system of claim 8, wherein the collision detect circuit includes an address compare circuit **[FIG. 1, elements 110, 120, and 123]** *that provides a match signal when the left port address and the right port address are the same;* **[Luo teaches this limitation, e.g. in column 4, lines 50-56, "If the two simultaneous addresses indicate a collision would occur in an access to the same address location, a same location signal SAME_LOC is activated, e.g., goes to a logic HIGH state for the duration of the collision of address**

signals. Otherwise, the same location signal SAME_LOC remains inactive, e.g., at a logic LOW state."] *a left port collision detect circuit that provides a left port collision signal when the match signal exists and when the right port is writing;* **[FIG. 1, elements 110, 120, and 123]** *a left port flip-flop that is set on the left port collision signal;* **[FIG.4 and associated text e.g.]** *a first left port latch that latches a collision flag from the left port flip-flop on a rising edge of a left port clock signal, wherein the left port flip-flop is reset according to the collision flag output from the first left port latch; a second left port latch that latches the collision flag from the first left port latch on a falling edge of the left port clock signal;* **[Luo discloses in column 5, lines 20-25, "...when a clock signal is at a logic HIGH), and the data is transferred, e.g., during the subsequent phase(0) (e.g., when the clock signal is at a logic LOW). Thus, when a collision is determined by the simultaneous access determination module 120 (e.g., when the same location SAME_LOC signal is activated)..."]** *and a left port output driver that provides the collision flag from the second left port latch."* **[FIG. 1, elements 110, 120, and 123] ["The first meta-stable wait state generator circuit 397 includes a meta-stable D-type Flip-Flop 310a (DFF), and the second meta-stable wait state generator circuit 399 includes another meta-stable DFF 310b." The examiner interprets a D Flip Flop as analogous to a latch. See FIGs. 3-4]**

With respect to **claim 10**,

"The system of claim 9, further including a flip-flop **[FIG. 4]** *that stores the left port address* **[FIG. 3]** *according to the left port collision signal* **[e.g. FIG. 3, "WAIT STATE 2"].** *"* **[Luo discloses this limitation as shown in FIGs. 3 and 4. Luo discloses in column 3, lines 9-11, "FIG. 4 shows an exemplary D-type Flip-Flop synchronizer capable of resolving meta-stable condition in the circuit shown in FIG. 3."]**

With respect to **independent claim 11**, and **claim 12**,

"A method of collision detection in a dual port memory system, comprising: detecting that a left port address to be presented to a left port is identical to a right port address to be presented to a right port; and generating a left port collision flag if a write operation is being processed for the right port address at the right port." **[Luo discloses in column 4, lines 57-61, "The asynchronous, simultaneous access wait state generator 123 generates a wait state signal WAIT STATE 1 relating to the first port of the dual port device, and a wait state signal WAIT STATE 2 relating to access from the second port of the dual port device. " Luo teaches this limitation, e.g. in column 4, lines 50-56.]**

With respect to **claim 13**,

"The method of claim 12, further including providing arbitration when either the left port collision flag or the right port collision tag is set." **[Luo discloses this limitation, e.g. in column 1, line 60 – column 2, line 6]**

With respect to **independent claim 14**,

> *"A method of collision detection, comprising: detecting an address match between two or more ports;* **[Luo teaches this limitation, e.g. in column 4, lines 50-56]** *and generating a collision flag* **["WAIT STATE"]** *for at least one of the two or more ports of any of the other of the two or more ports are writing."* **[Luo discloses in column 4, lines 57-61, "The asynchronous, simultaneous access wait state generator 123 generates a wait state signal WAIT STATE 1 relating to the first port of the dual port device, and a wait state signal WAIT STATE 2 relating to access from the second port of the dual port device. " Luo teaches this limitation, e.g. in column 4, lines 50-56.]**

With respect to **independent claim 15**,

> *"A method of collision detection, further comprising: providing arbitration when the collision flag is set."* **[Luo discloses this limitation, e.g. in column 1, line 60 – column 2, line 6]**

CONCLUSION

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571)

272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Reginald G. Bragdon

Horace L. Flournoy

Patent Examiner

Art unit: 2189

Supervisory Patent Examiner

Technology Center 2100

DETAILED ACTION

REASONS FOR ALLOWANCE

This Office Action has been issued in response to the remarks filed March 20th 2007. Applicant's arguments have been carefully and respectfully considered, and are persuasive to the examiner.

The following is an examiner's statement of reasons for allowance:

Independent claims 1, 8, 11, and 14 are allowable over the prior art of record for the remarks to each independent claim as set forth on pages 2-4 of the response received 3/20/2007. As such, each of the dependent claims is allowable.

Additionally the limitations, or iterations thereof found in each independent claim, of *"...wherein the collision detect circuit sets a collision flag when a collision condition is detected in any of the at least two ports, the collision flag providing an indication that any of the at least two ports may have read or written corrupted data."* in combination with all other limitations found in each of the independent claims present claims 1, 8, 11 and 14 in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance.

Relevant Prior Art Cited by the Examiner

United States Patent No. 6,915,400 (Engelahardt) discloses in column 1, lines 34-36 (also column 1, lines 42-46) teachings that appear similar to the claim language of *"...wherein the collision detect circuit sets a collision flag when a collision condition is detected in any of the at least two ports" found* in the instant application. However, Engelahardt does not disclose this teaching in combination with all other limitations found in each of the independent claims.

CONCLUSION

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Reginald G. Bragdon

Reginald G. Bragdon

HLF
April 5th, 2007

Supervisory Patent Examiner
Technology Center 2100

Notice of References Cited

Application/Control No.	Applicant(s)/Patent Under Reexamination	
10/808,253	YEH ET AL.	
Examiner	Art Unit	Page 1 of 1
Horace L. Flournoy	2189	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0068633	04-2004	Engelahardt, Markus	711/167
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,253	03/23/2004	Tzong-Kwang Henry Yeh	9145.0021-00	4222

22852 7590 05/01/2007

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EXAMINER	
FLOURNOY, HORACE L	
ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 05/01/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 211 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 211 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability

Application No.	Applicant(s)	
10/808,253	YEH ET AL.	
Examiner	**Art Unit**	
Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *after final response received 3/20/2007*.

2. ☒ The allowed claim(s) is/are *1-15*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☒ Certified copies of the priority documents have been received in Application No. *60/548,527* .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.